FIG.1

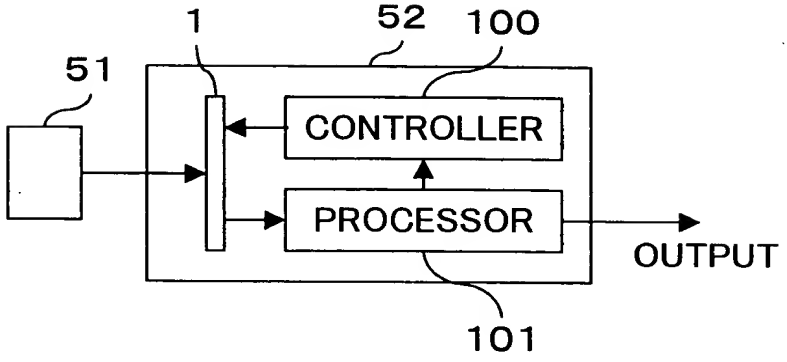

1
52
100
51
CONTROLLER
PROCESSOR
OUTPUT
101

FIG.2

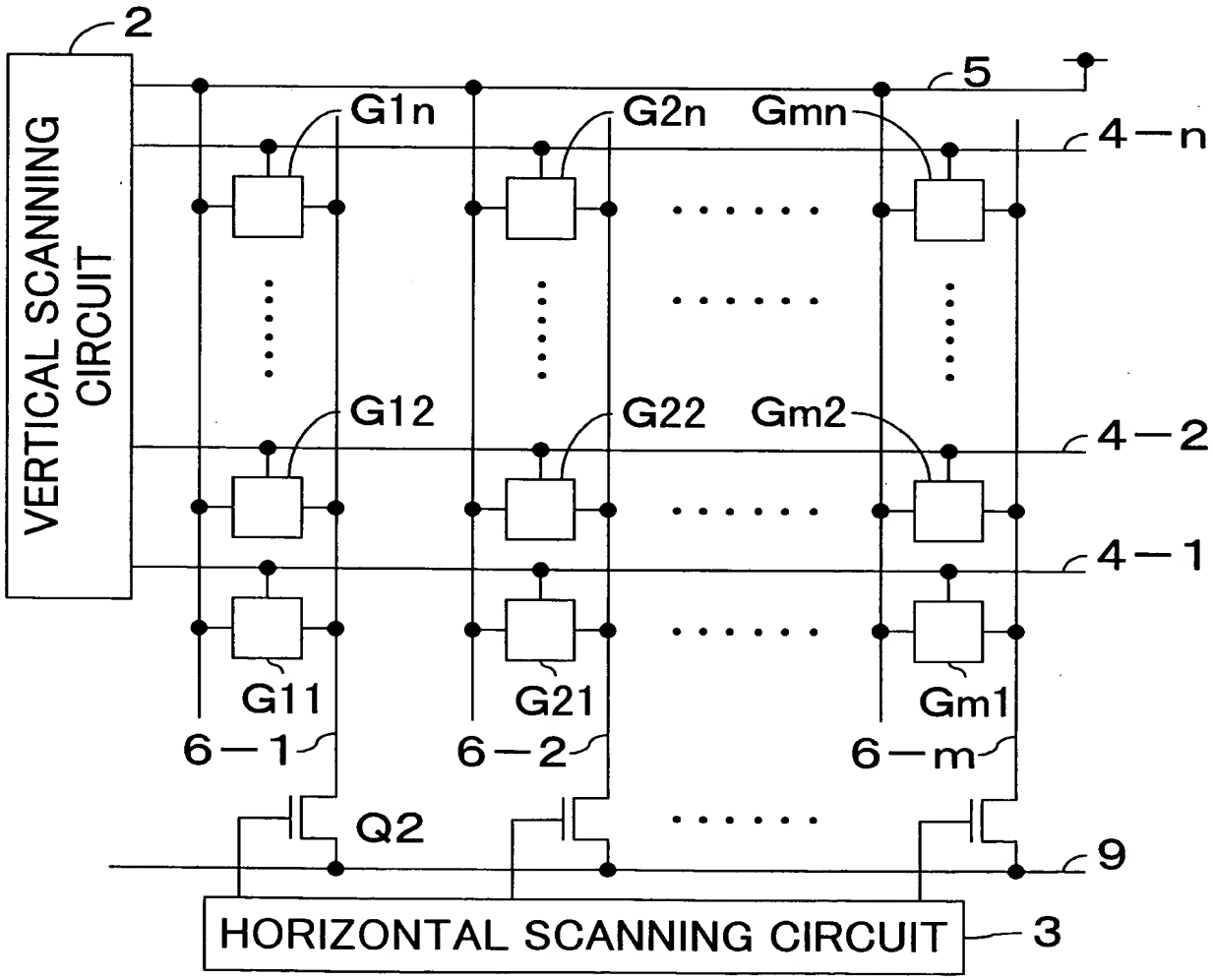

2
VERTICAL SCANNING CIRCUIT
5
G1n
G2n
Gmn
4—n
G12
G22
Gm2
4—2
4—1
G11
G21
Gm1
6—1
6—2
6—m
Q2
9
HORIZONTAL SCANNING CIRCUIT
3

FIG.3

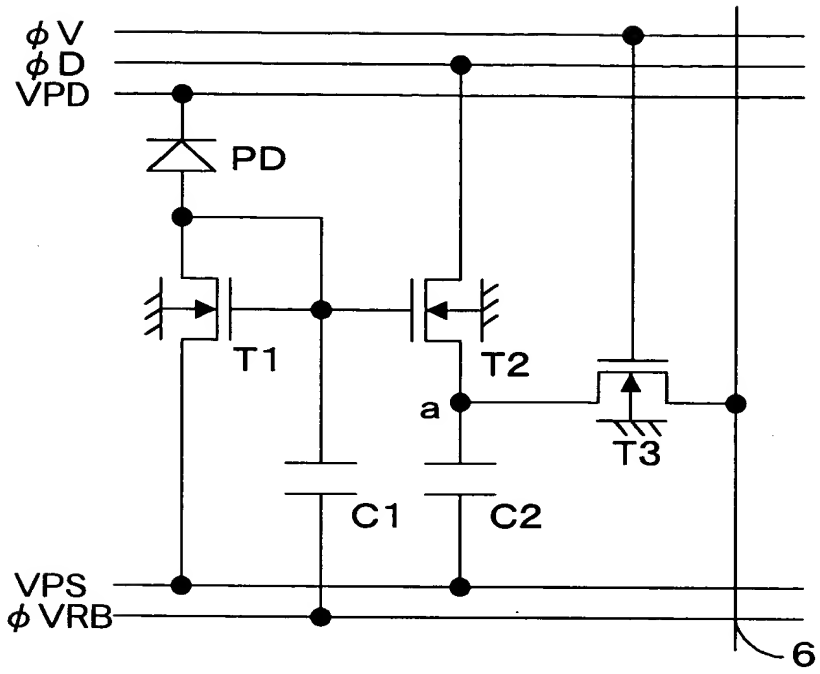

φV
φD
VPD
PD
T1
T2
a
T3
C1
C2
VPS
φVRB
6

FIG.4

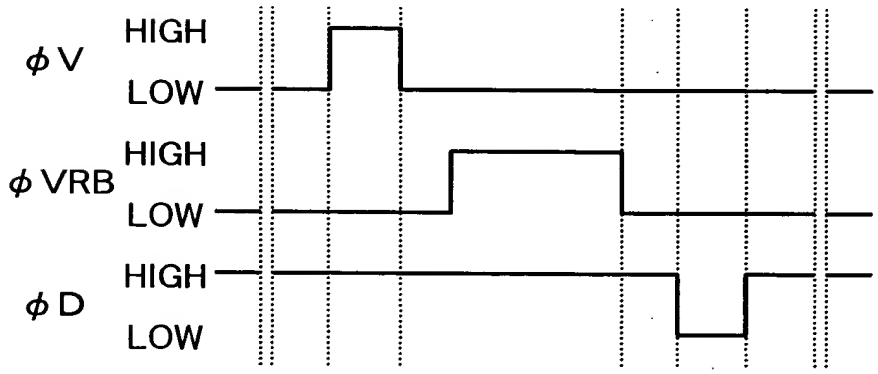

φV
HIGH
LOW
φVRB
HIGH
LOW
φD
HIGH
LOW

FIG.5A

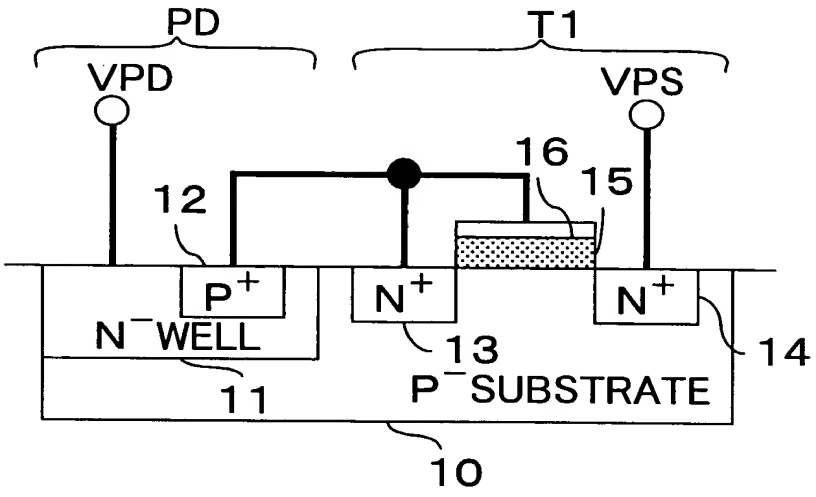


FIG.5B

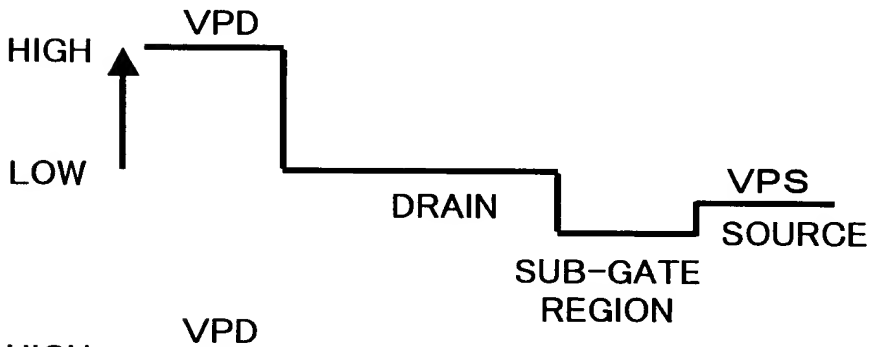


FIG.5C

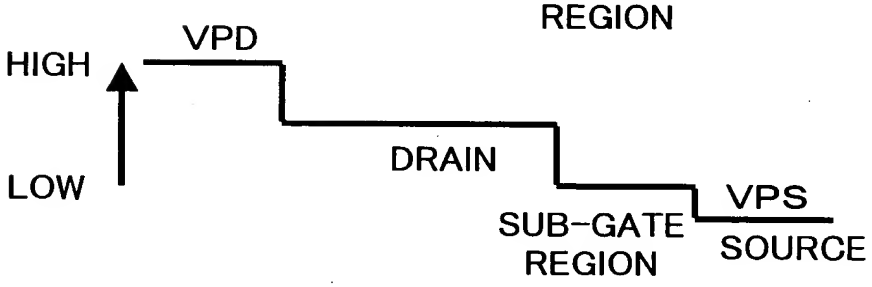


FIG.5D

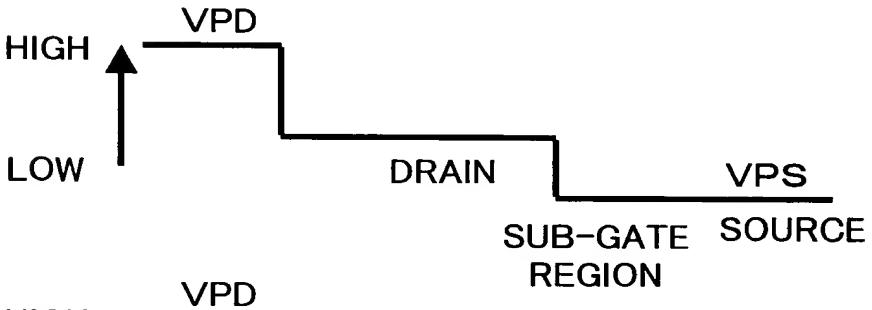


FIG.5E

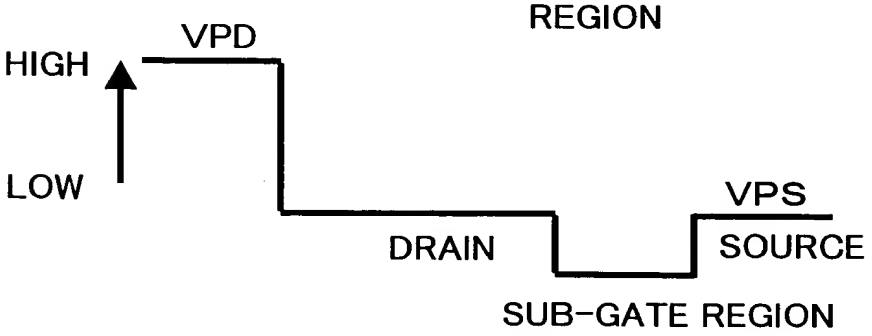


FIG.6

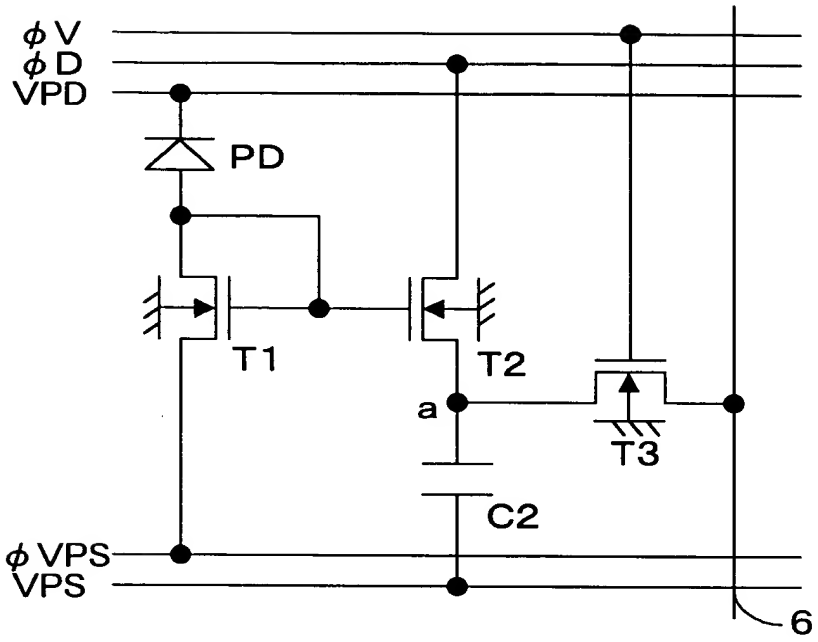

φV
φD
VPD
PD
T1
T2
a
T3
C2
φVPS
VPS
6

FIG.7

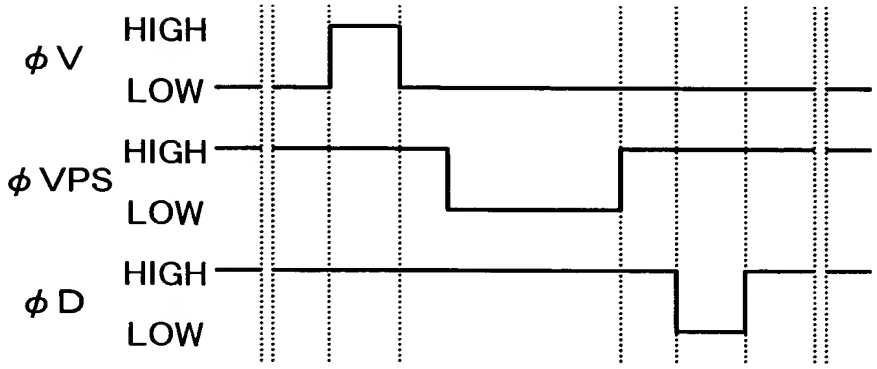

φV
HIGH
LOW
φVPS
HIGH
LOW
φD
HIGH
LOW

FIG.8A

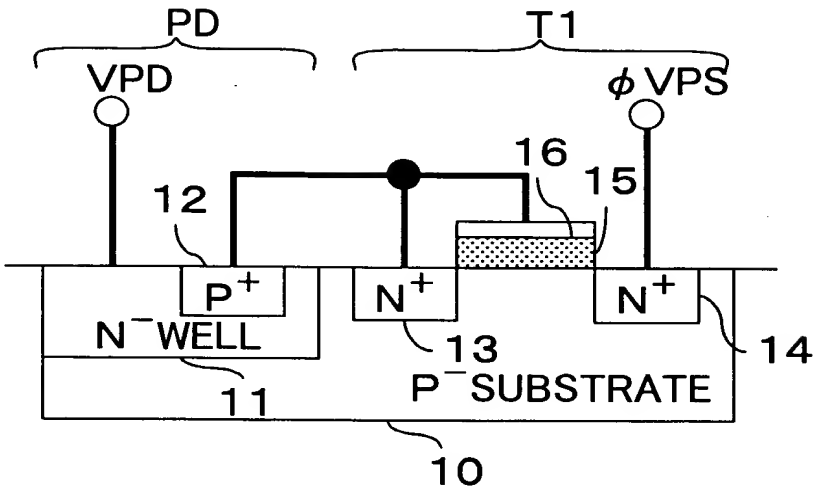


FIG.8B

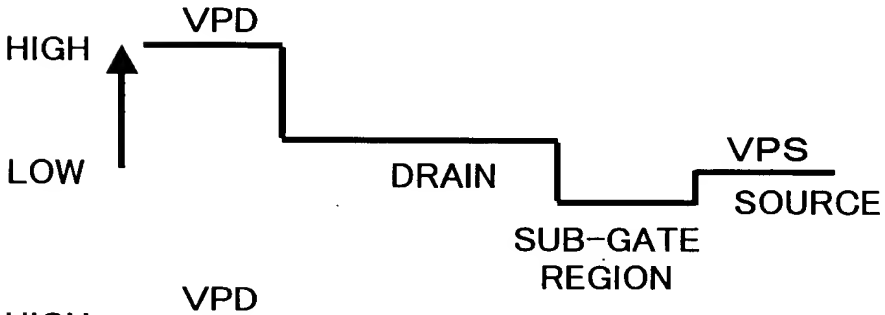


FIG.8C

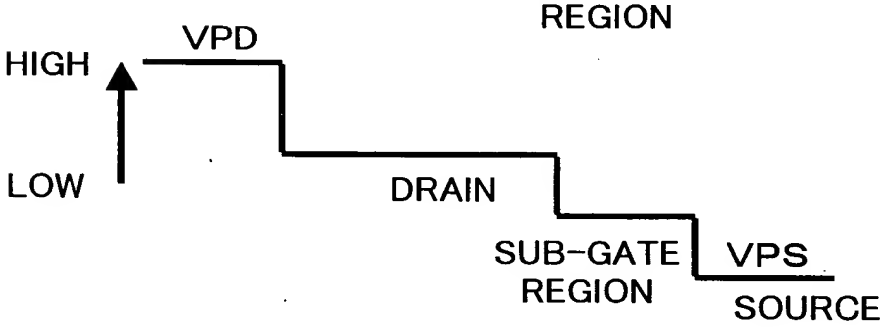


FIG.8D

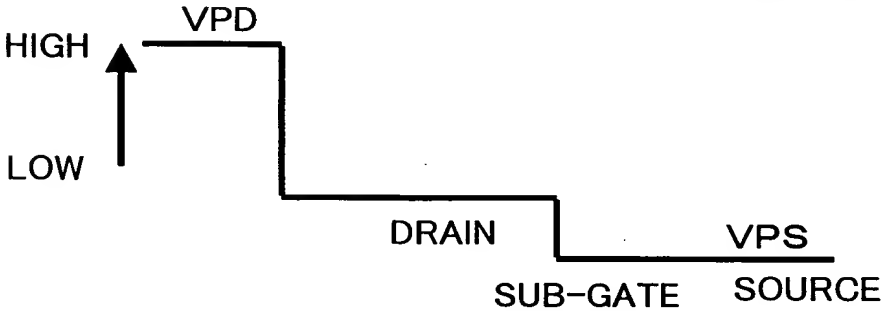


FIG.8E

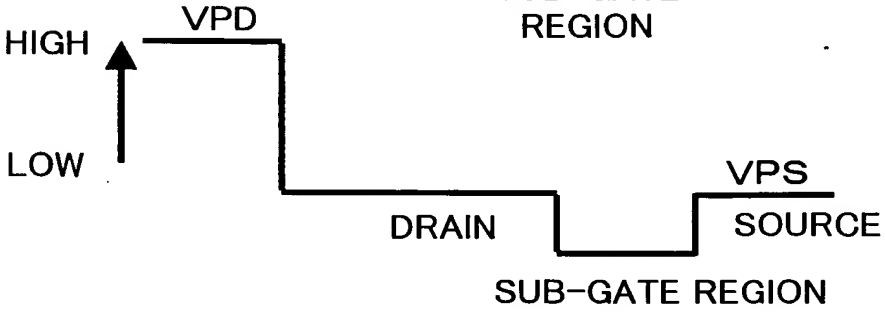


FIG.9

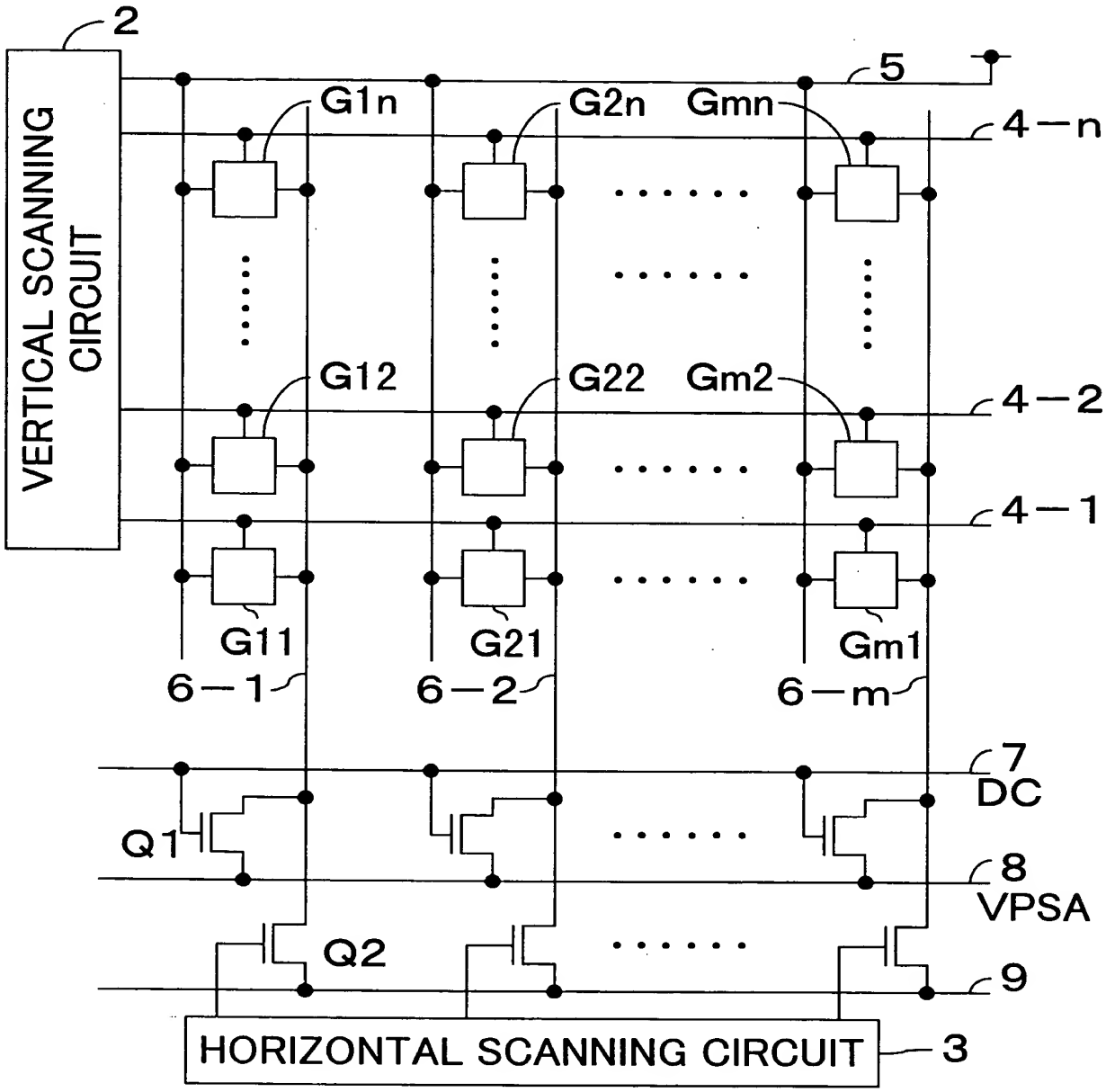

2
VERTICAL SCANNING CIRCUIT
5
G1n
G2n
Gmn
4—n
G12
G22
Gm2
4—2
4—1
G11
G21
Gm1
6—1
6—2
6—m
7
DC
Q1
8
VPSA
Q2
9
HORIZONTAL SCANNING CIRCUIT
3

FIG.10A

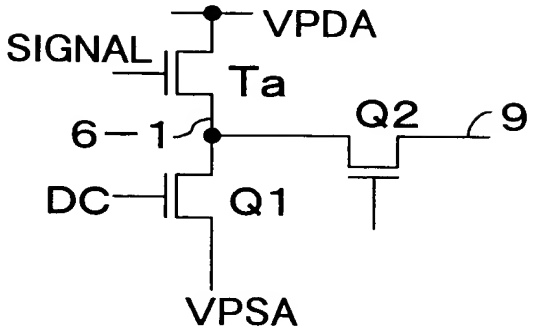


FIG.10B

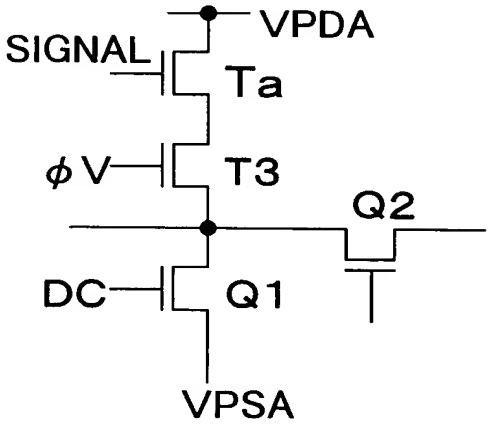


FIG.11

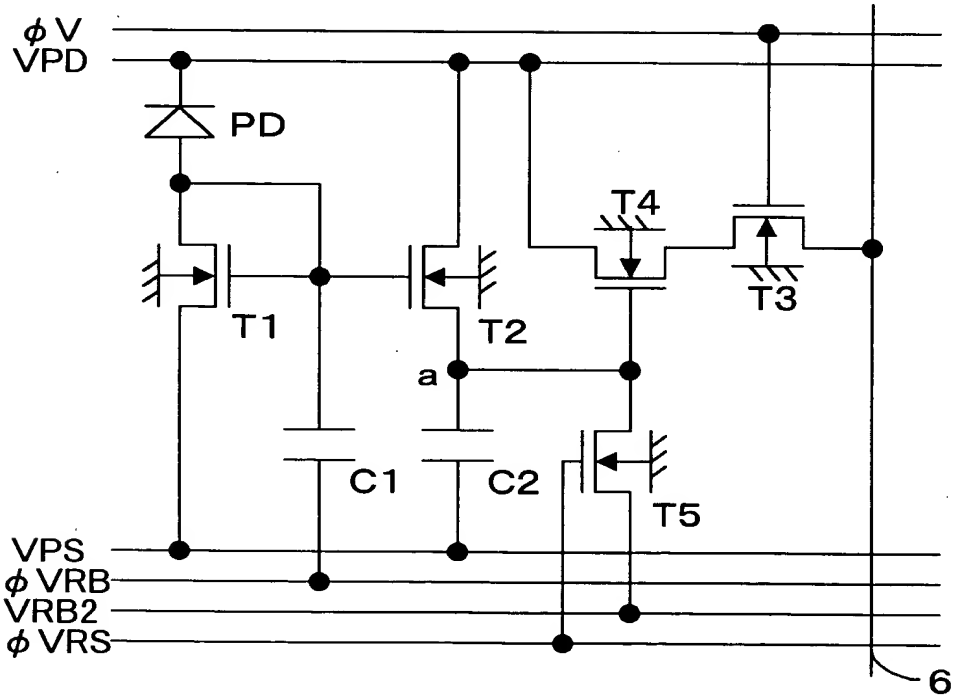


FIG.12

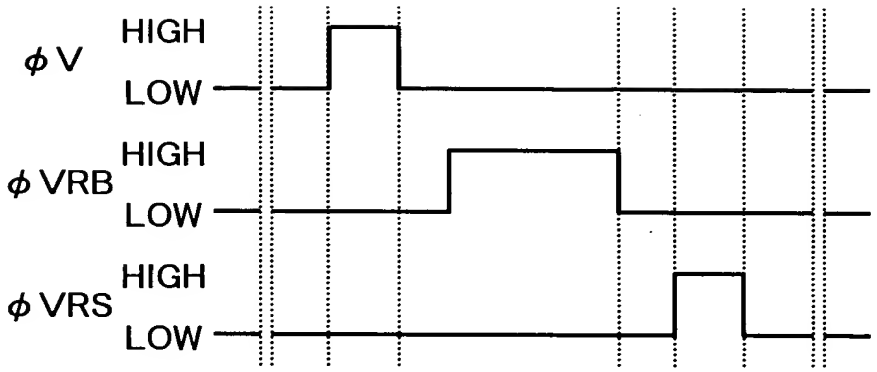

φV
HIGH
LOW
φVRB
HIGH
LOW
φVRS
HIGH
LOW

FIG.13

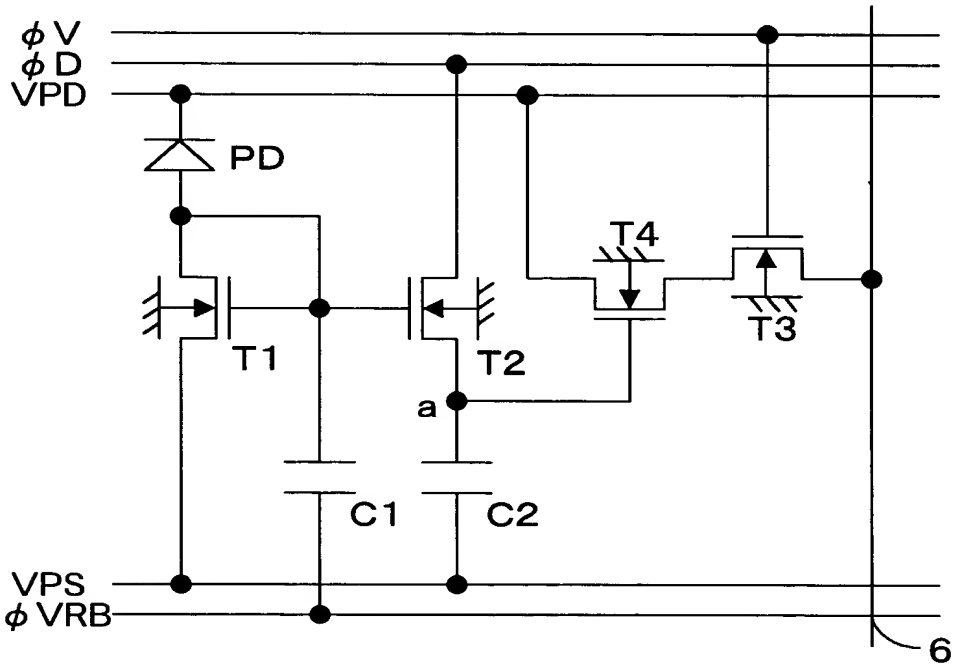

φV
φD
VPD
PD
T1
T2
T3
T4
a
C1
C2
VPS
φVRB
6

FIG.14

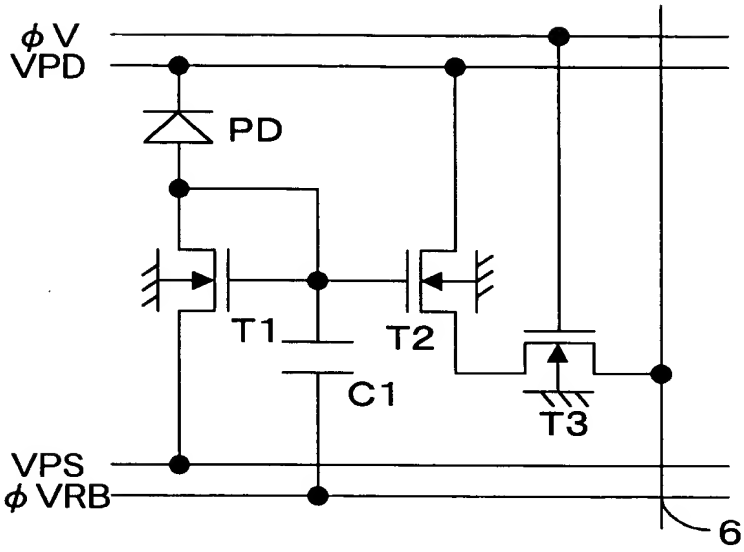
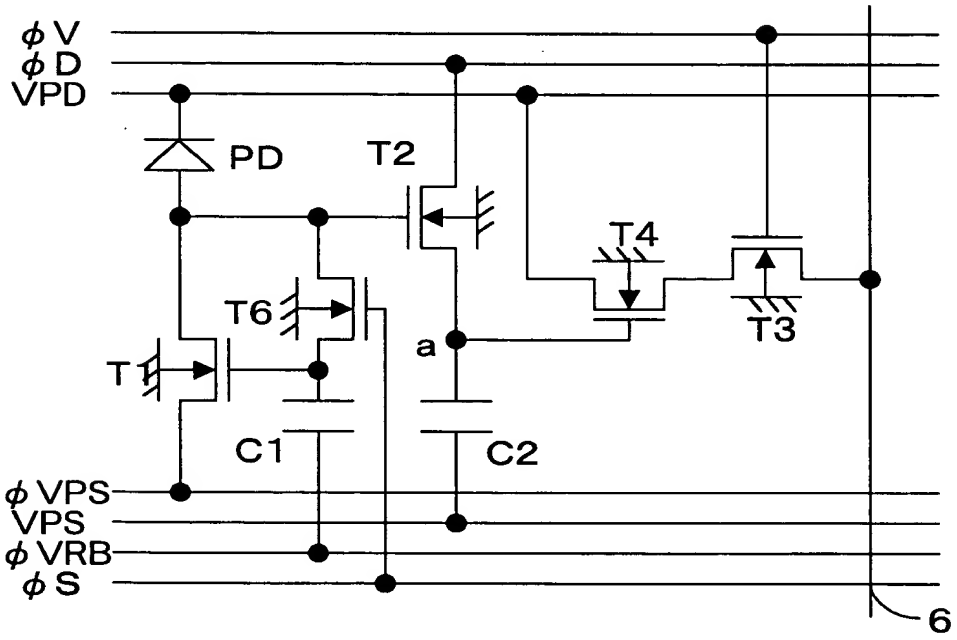

φV
VPD
PD
T1
T2
C1
T3
VPS
φVRB
6

FIG.15


φV
φD
VPD
PD
T2
T4
T6
T3
a
T1
C1
C2
φVPS
VPS
φVRB
φS
6

0087-20 92E8T960

FIG.16

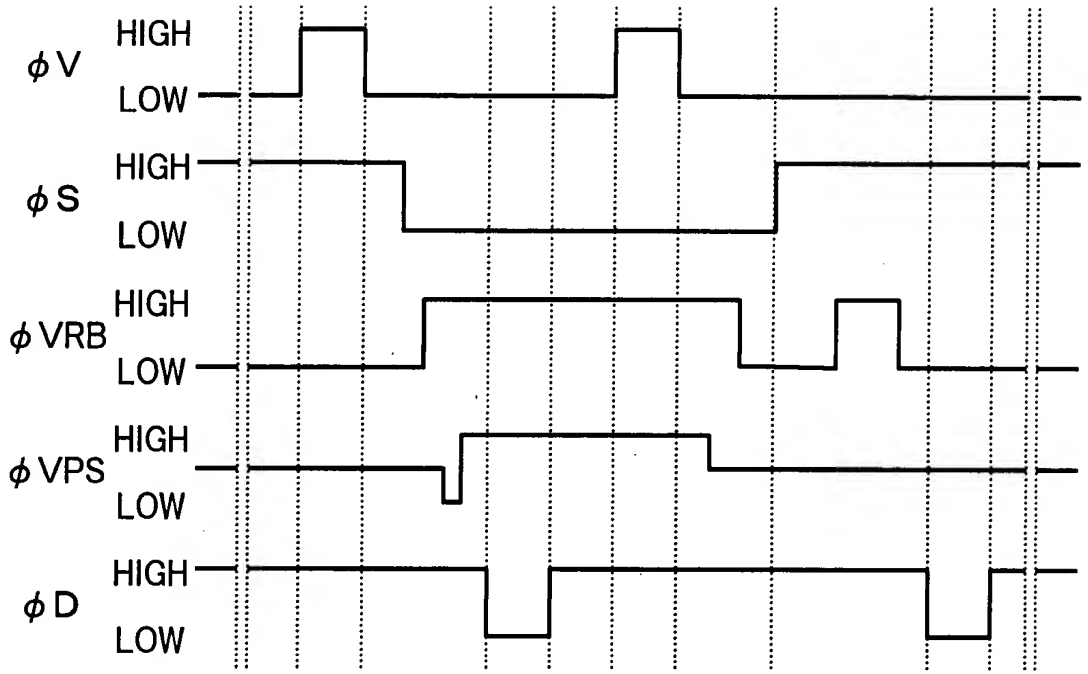


FIG.17A

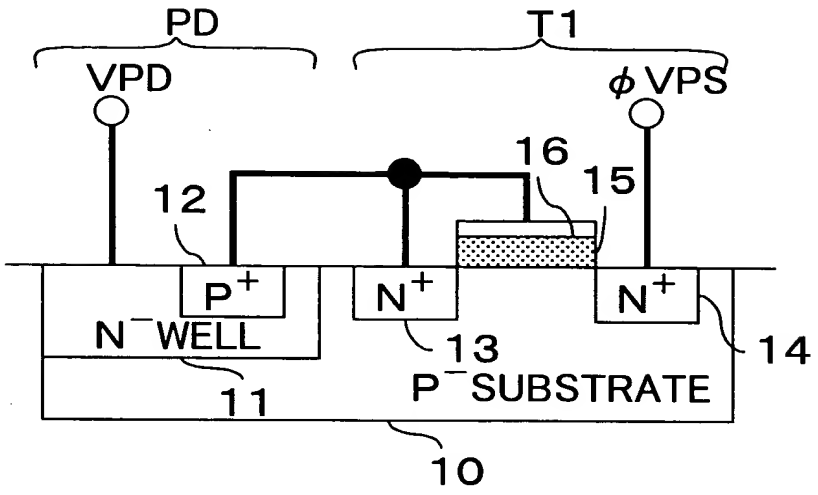


FIG.17B

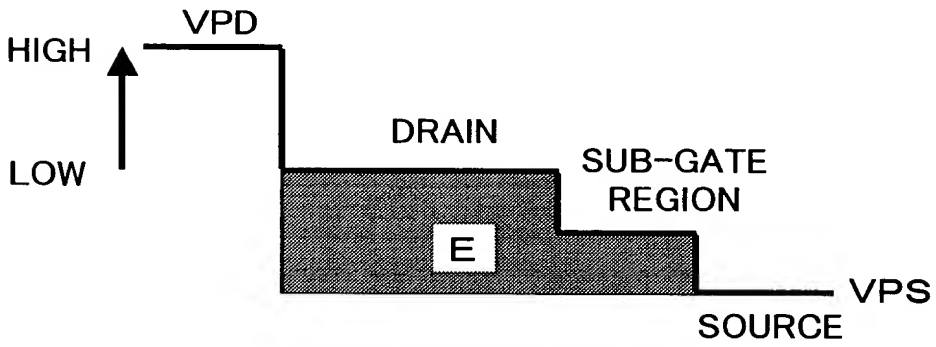


FIG.17C

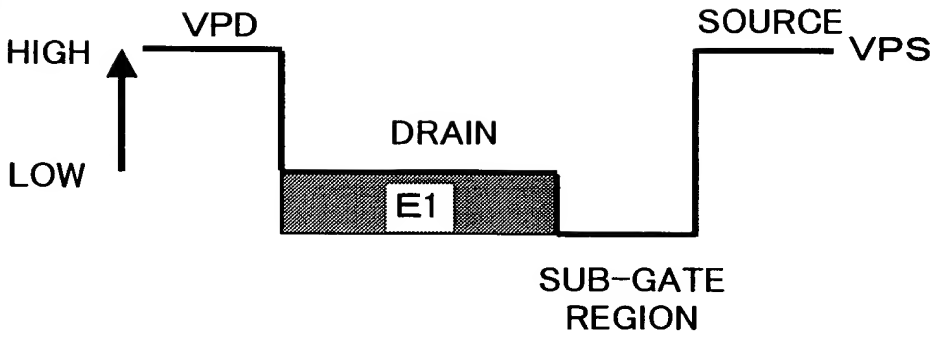


FIG.18

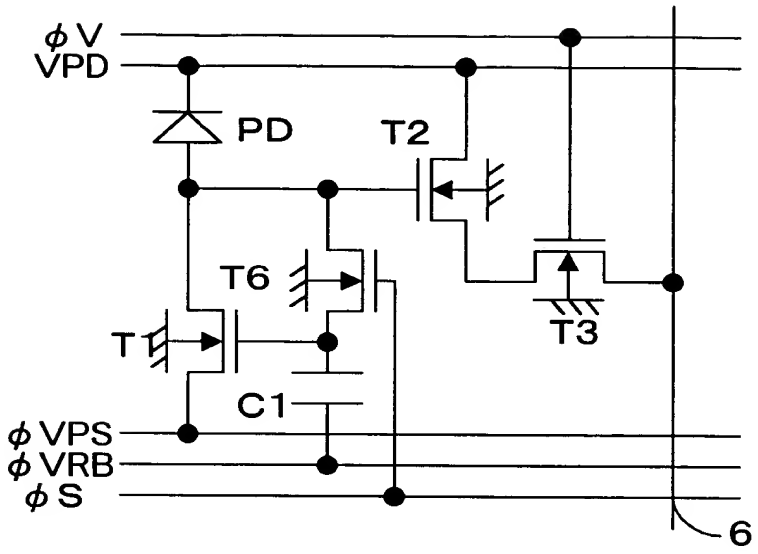

φV
VPD
PD
T2
T6
T3
T1
C1
φVPS
φVRB
φS
6

FIG.19

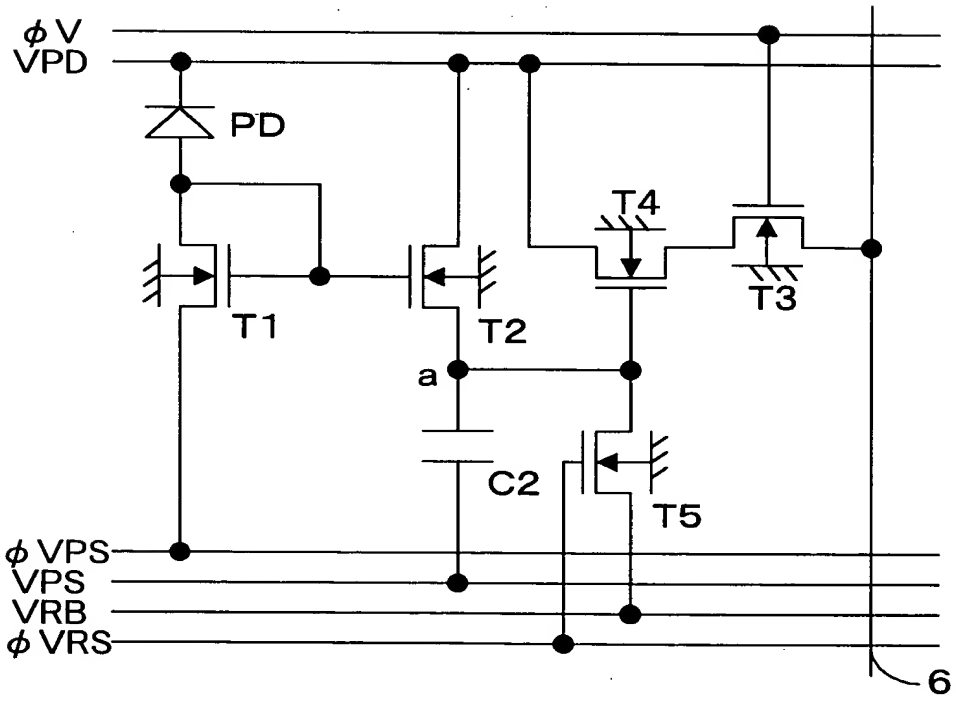

φV
VPD
PD
T4
T3
T1
T2
a
C2
T5
φVPS
VPS
VRB
φVRS
6

FIG.20

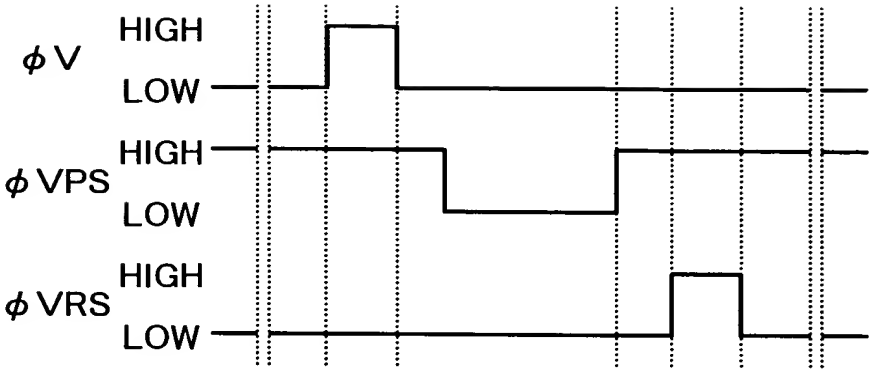

φV
HIGH
LOW
φVPS
HIGH
LOW
φVRS
HIGH
LOW

FIG.21

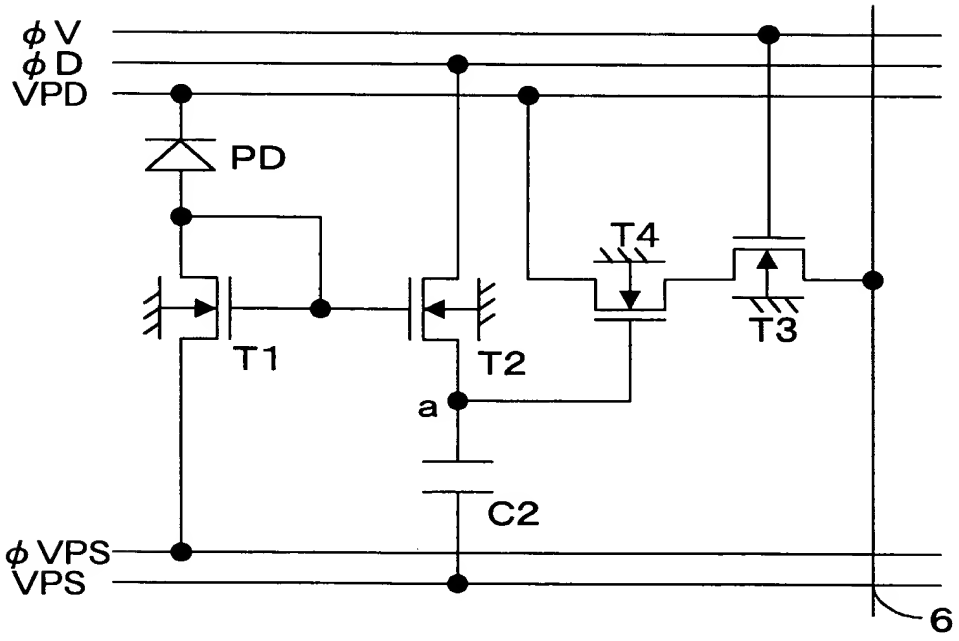

φV
φD
VPD
PD
T4
T1
T2
T3
a
C2
φVPS
VPS
6

FIG.22

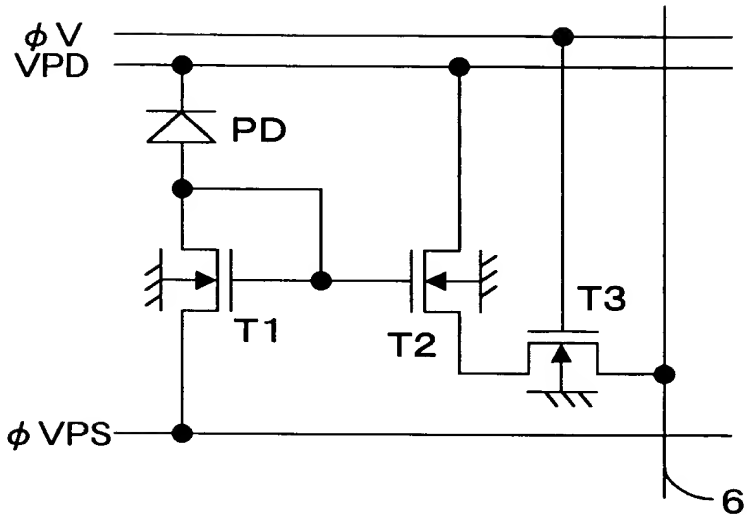


FIG.23

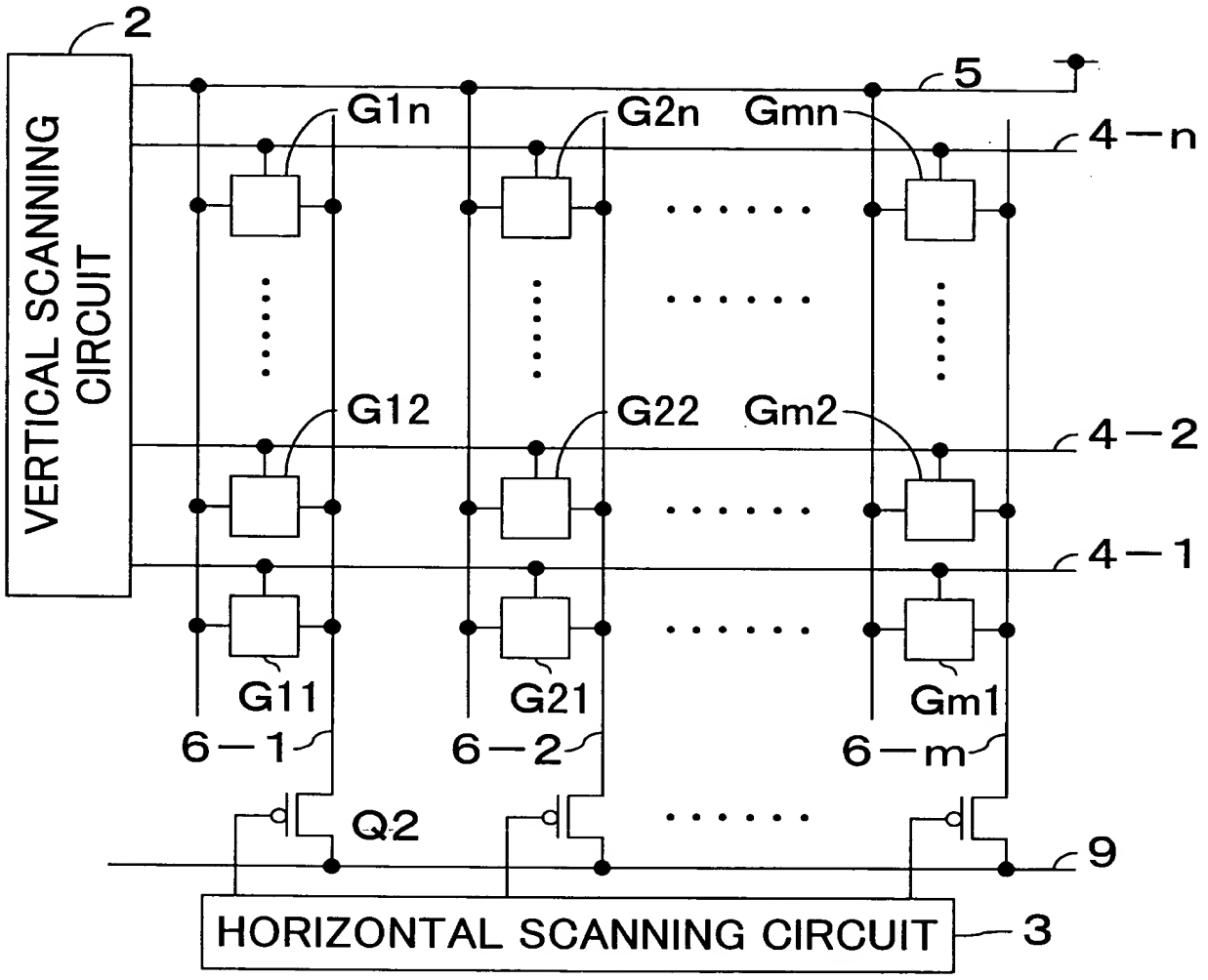

2
VERTICAL SCANNING CIRCUIT
5
G1n
G2n
Gmn
4—n
G12
G22
Gm2
4—2
4—1
G11
G21
Gm1
6—1
6—2
6—m
Q2
9
HORIZONTAL SCANNING CIRCUIT
3

FIG.24

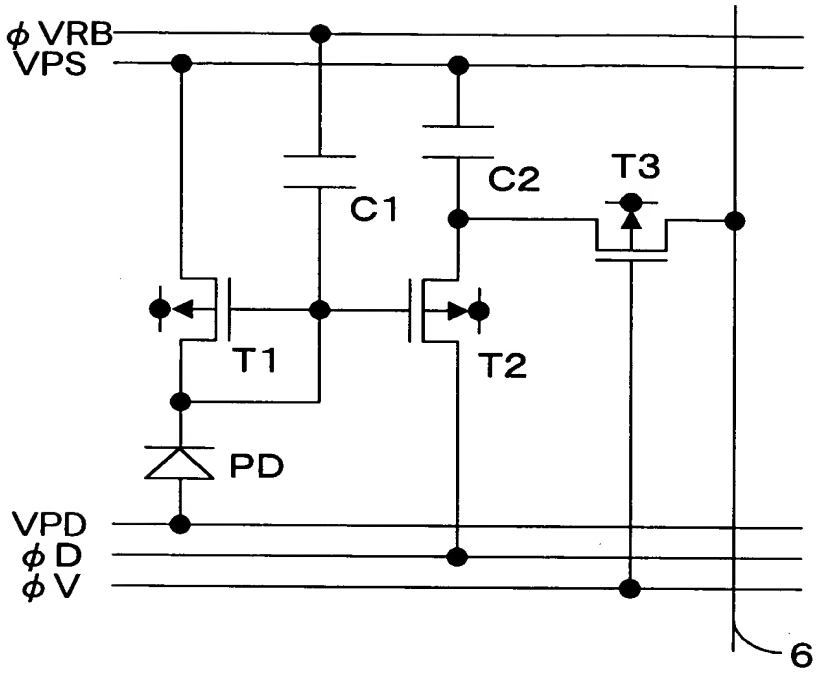

φVRB
VPS
C1
C2
T3
T1
T2
PD
VPD
φD
φV
6

FIG.25

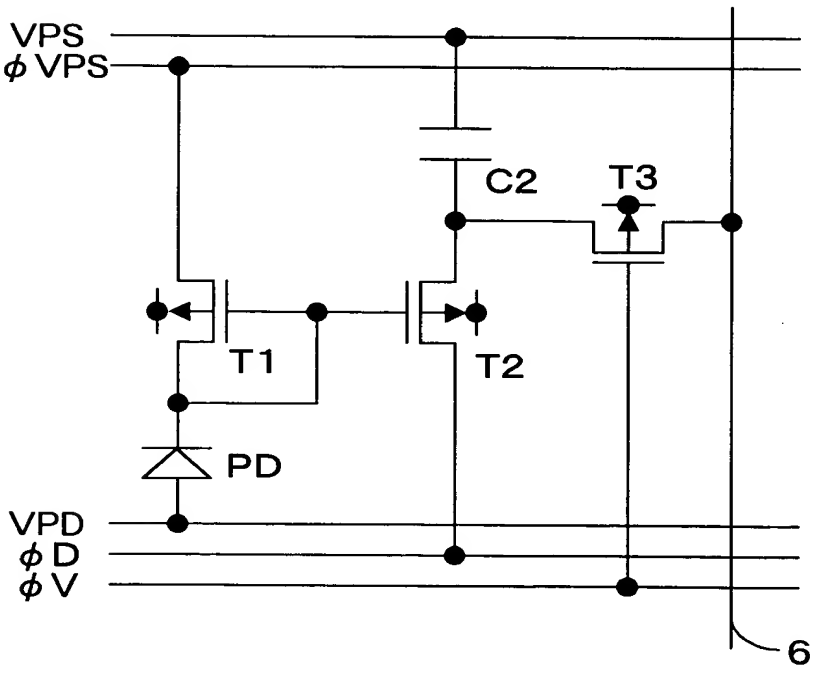

VPS
φVPS
C2
T3
T1
T2
PD
VPD
φD
φV
6

FIG.26

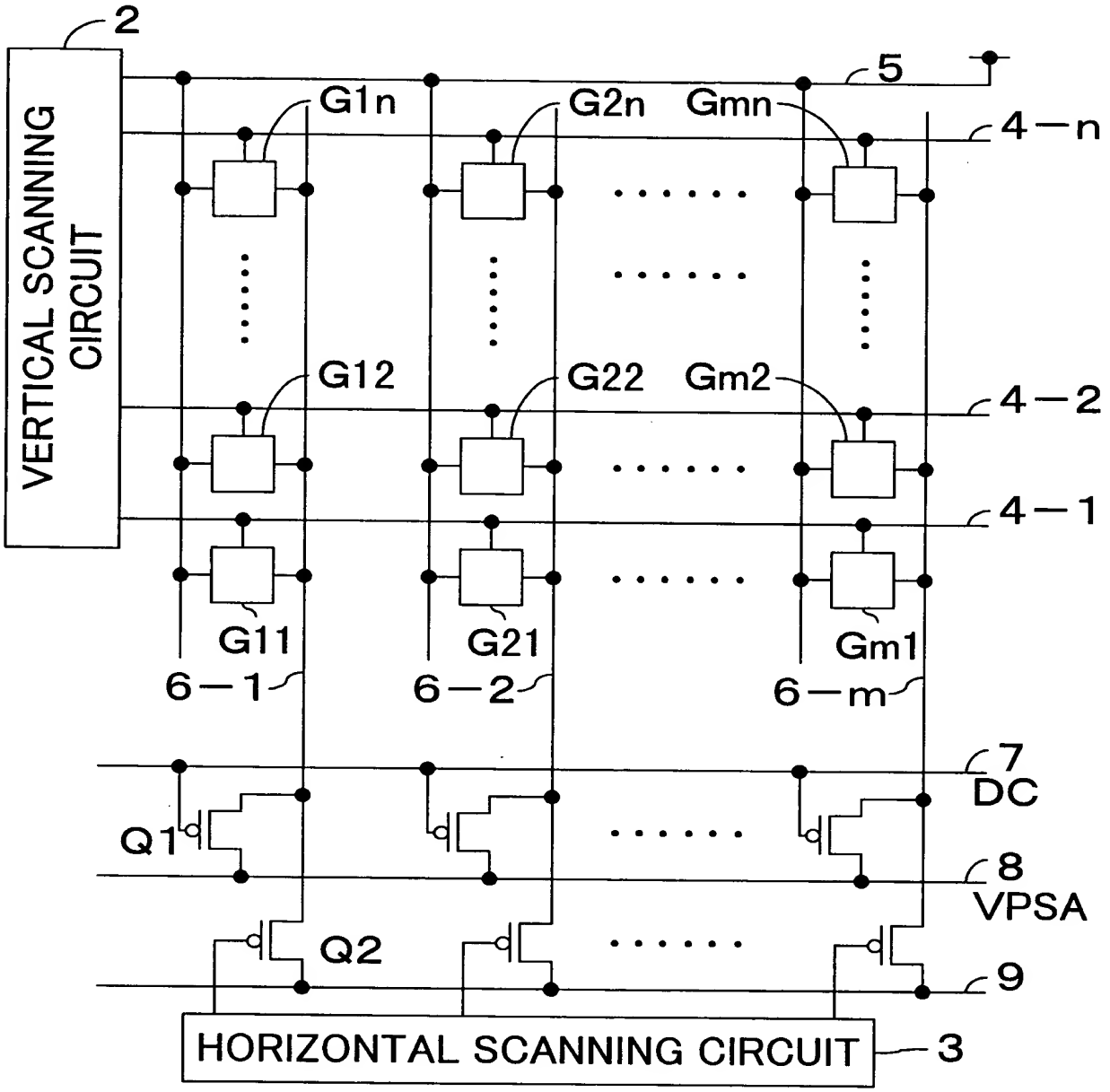

2
VERTICAL SCANNING CIRCUIT
5
G1n
G2n
Gmn
4−n
G12
G22
Gm2
4−2
4−1
G11
G21
Gm1
6−1
6−2
6−m
7
DC
Q1
8
VPSA
Q2
9
HORIZONTAL SCANNING CIRCUIT
3

FIG.27A

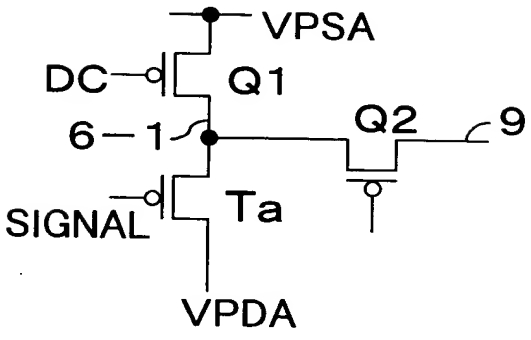


FIG.27B

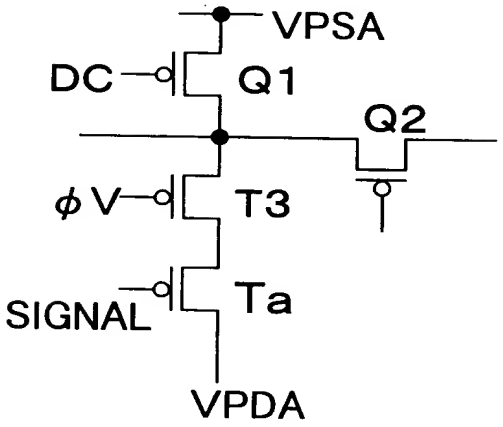


FIG.28

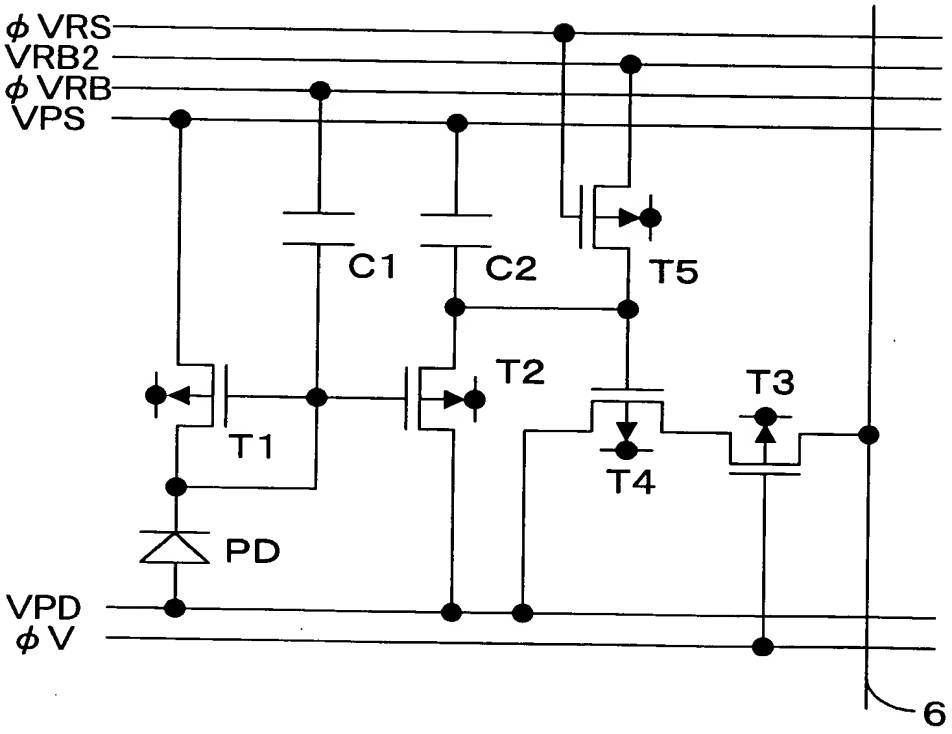


FIG.29

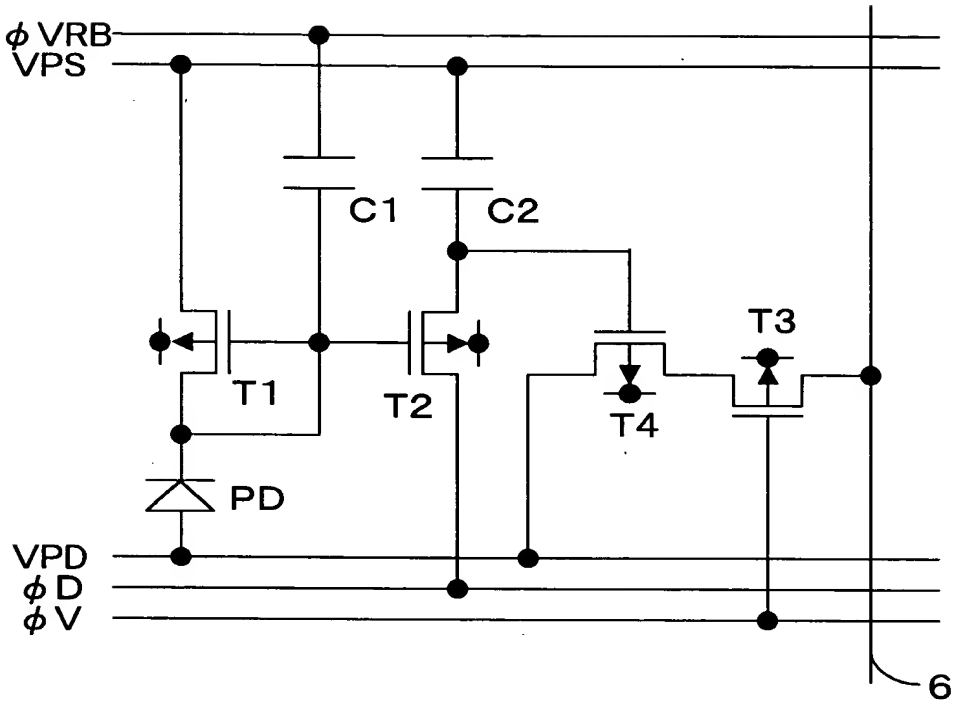

φVRB
VPS
C1
C2
T1
T2
T3
T4
PD
VPD
φD
φV
6

FIG.30

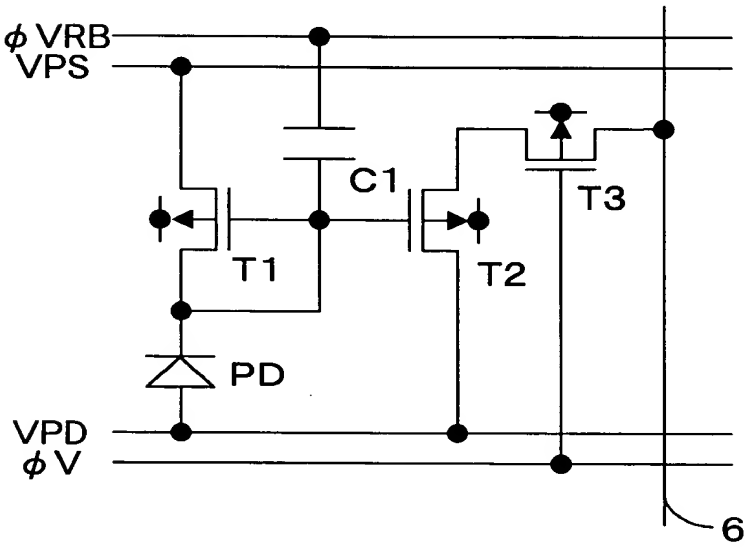

φVRB
VPS
C1
T1
T2
T3
PD
VPD
φV
6

FIG.31

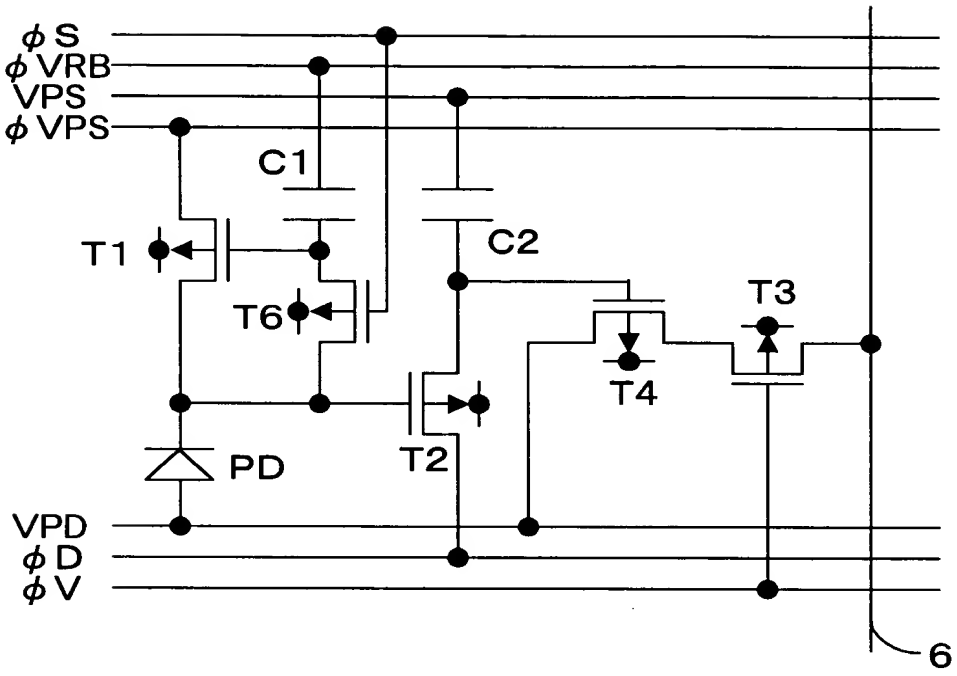

φS
φVRB
VPS
φVPS
C1
C2
T1
T6
T3
T4
PD
T2
VPD
φD
φV
6

FIG.32

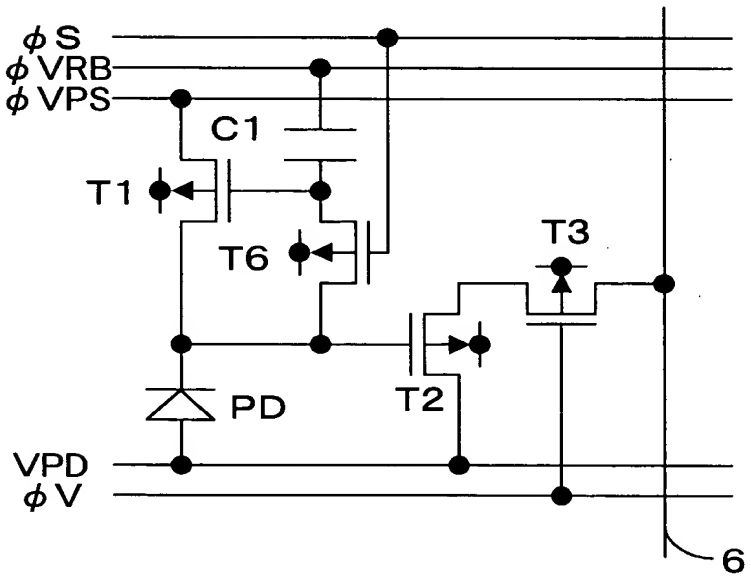

φS
φVRB
φVPS
C1
T1
T6
T3
PD
T2
VPD
φV
6

FIG.33

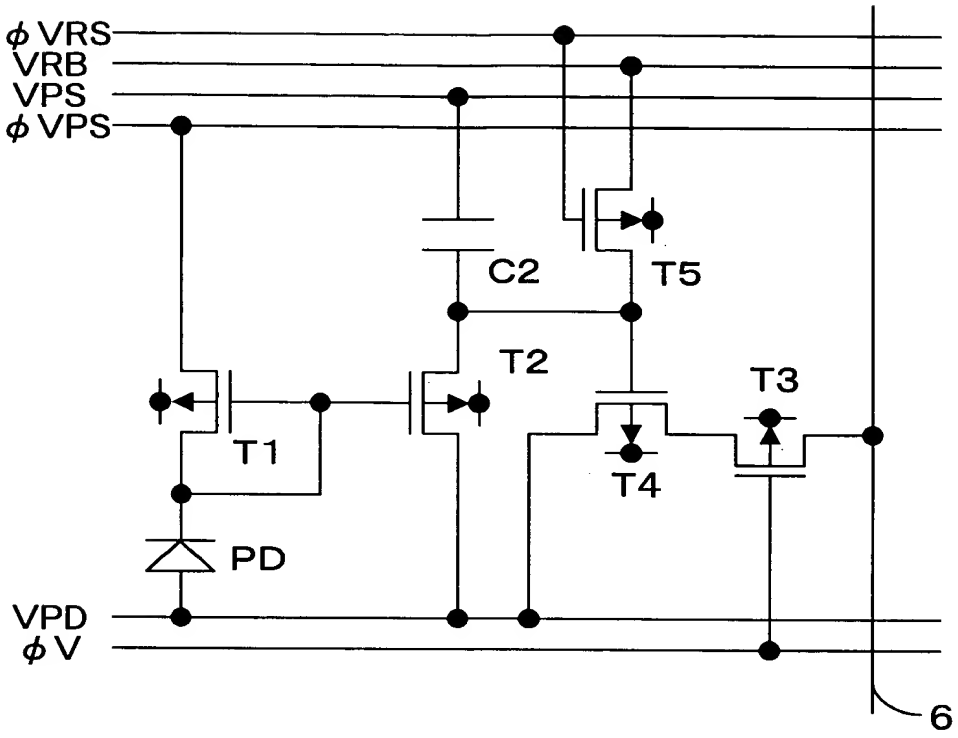

φVRS
VRB
VPS
φVPS
C2
T5
T2
T3
T1
T4
PD
VPD
φV
6

FIG.34

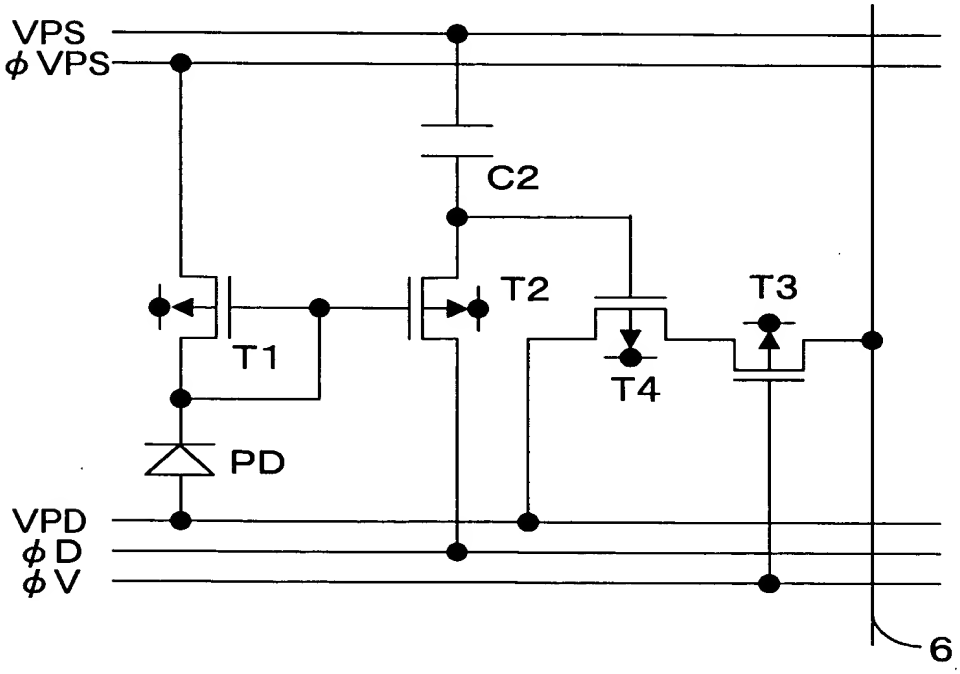

VPS
φVPS
C2
T2
T3
T1
T4
PD
VPD
φD
φV
6

FIG.35

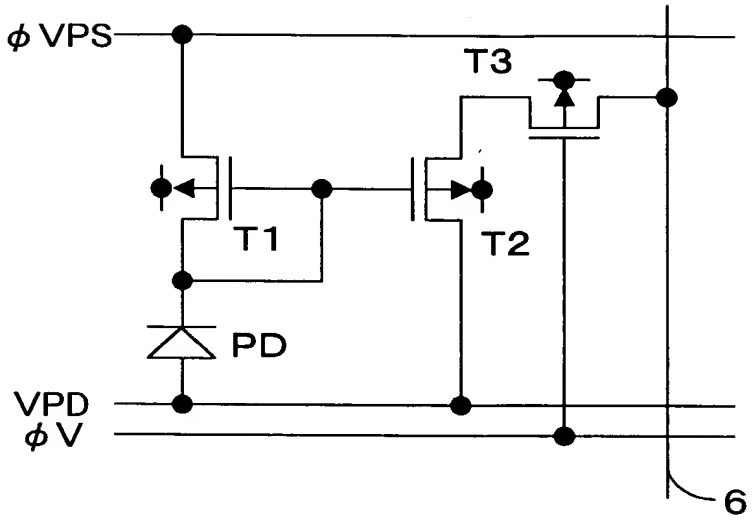

φVPS
T3
T1
T2
PD
VPD
φV
6

FIG.36

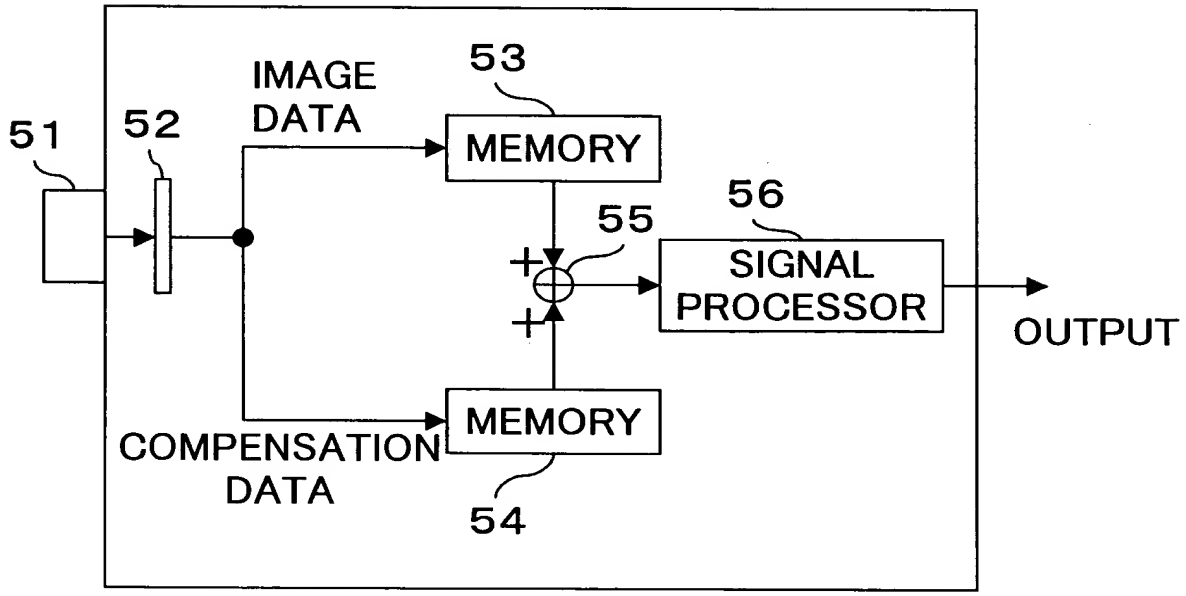
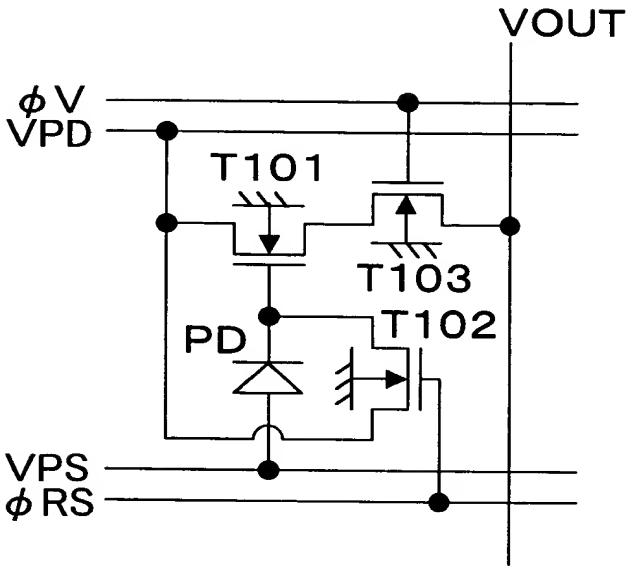

51
52
IMAGE DATA
53
MEMORY
56
55
SIGNAL PROCESSOR
OUTPUT
MEMORY
COMPENSATION DATA
54

FIG.37

PRIOR ART